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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/868,773

06/21/2001

Andreas Jurisch

449122006400

6177

25227 7590 09/19/2006

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EXAMINER

ZHENG, EVA Y

ART UNIT

PAPER NUMBER

2611

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/868,773

Applicant(s)

JURISCH, ANDREAS

Examiner

Eva Yi Zheng

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### *Request for Continued Examination*

1. The request filed on July 12, 2006, for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 09/868,773 is acceptable and a RCE has been established. An action on the RCE follows.

### *Response to Arguments*

2. Applicant's arguments filed July 12, 2006 have been fully considered but they are not persuasive. Examiner has thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meet the claimed limitation as rejected.

Applicant's argument – Prior art by Borazani failed to disclose a single resampling device.

Examiner's response – It is well known that a device may refers to a machine that consists of multiple components, not limit to just one. A single device may interpret as multiple identical components that constitute as a single device. Borazani et al teach a multi-channel modulating system comprise a plurality of input signals and upsampling to higher frequencies (120 in Fig. 8, Col 20, L55-68). Although block 120 has a set of same upsampler, it performs the same task as a single upsampler. Whether to have two upsamplers or embodied to only one upsampler produce no new or unexpected result, so long as to produce upsampling of the input signals. Therefore, it is obvious to one of ordinary skill in the art to implement the upsampling device by

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Borazjani et al in the digital signal synchronization system of Lew et al. By doing so, reduce cost, reduce system in size, and produce desire signals in a communication system.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lew et al. (WO 92/17951) (IDS) in view of Borazjani et al (US 5,825,829).

a) Regarding to claim 1, Lew et al. disclose a method for synchronizing a plurality of digital input signals, which are each formed by sampling with a dedicated operating clock (54 and 55 in Fig. 3), comprising:

forming digital auxiliary signals by sampling the digital input signals with a post-processing clock (65 and 66 in Fig. 3); which is at least twice as fast as the fastest operating clock (page 9, L10-15); and

forming synchronized digital output signals (59 and 60 in Fig. 3) which correspond to the digital input signals by interpolating each digital auxiliary signal (110 and 112 in Fig. 3; page 9, L6-9).

Lew et al. disclose all of the subject matters above except for the specific teaching of using only one resampling device. However, Borazjani et al teach a multi-

channel modulating system comprise a plurality of input signals and upsampling to higher frequencies (120 in Fig. 8, Col 20, L55-68). It is well known that resampling is also called sample rate conversion, that convert a sampled signal from one sampling frequency to another, which has the same functionality as upsampler. In addition, although block 120 has a set of same upsampler, it performs the same task as a single upsampler. Therefore, it is obvious to one of ordinary skill in the art to implement the upsampling device by Borazjani et al in the digital signal synchronization system of Lew et al. By doing so, reduce cost, reduce system in size, and produce desire signals in a communication system.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being obvious over Lew et al. (WO 92/17951) (IDS) in view of Borazjani et al (US 5,825,829), further in view of Yen et al. (US 4,707,841).

a) Regarding to claim 2, Lew et al. and Borazjani et al disclose all the subject matters described above except for the specific teaching of an inverse interpolation filter.

However, Yen et al., disclose converting to digital signals and coupled to an inverse interpolation filter (as shown in Fig.1). Therefore, it is obvious to one of ordinary skill in art to combine the inverse interpolation filter by Yen et al. in the system of Lew et al and Borazjani et al. By doing so, correct signal timing and better synchronization performance.

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6. Claim 3 is rejected under 35 U.S.C. 103(a) as being obvious over Lew et al. (WO 92/17951) (IDS) in view of Borazjani et al (US 5,825,829), further in view of Menkhoff et al. (US 6,137,349).

Regarding to claim 3, Lew et al. and Borazjani et al disclose all the subject matters described above except for the specific teaching of anti-aliasing filter directly after the interpolation.

However, Menkhoff et al. disclose filtering the synchronized digital output signals with an anti-alasing filter directly after the interpolation (3 in Fig.1).

Therefore, it is obvious to one of ordinary skill in art to implement the teaching of applying anti-alasing filter directly after the interpolation by Menkhoff et al. in the in the system of Lew et al and Borazjani et al. By doing so, reduce sampling rate and output desired signals in a high speed communication system.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lew et al. (WO 92/17951) (IDS) in view of Borazjani et al (US 5,825,829), in further view of Ley et al. (US 6,594,613).

Regarding to claim 4, Lew et al. and Borazjani et al disclose all the subject matters above except for the specific teaching of signals are obtained from secondary variable of measuring transducers in an electric power supply system.

However, Ley et al, disclose an adjustable bandwidth system comprise a sensor which sense secondary variable and filtering based on secondary variable (53 in Fig. 3). Therefore, it is obvious to one of ordinary skill in art to implement a secondary variable

sensor in the teaching of Ley et al with the digital signal synchronization system of Lew et al and Borazjani et al. By doing so, automatically adjust noise and reduce unwanted signals in a communication system.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lew et al. (WO 92/17951) (IDS) in view of Borazjani et al (US 5,825,829), in further view of Ley et al. (US 6,594,613), and further in view of Camp et al. (US, 5,592,517).

Regarding to claim 5, Lew et al., Borazjani et al, and Ley et al. disclose all the subject matters above except for the specific teaching of using an integrator for the interpolation.

However, Camp et al., disclose a cascaded integrator interpolating filters (as shown in Fig. 2). A digital interpolating filter increases the sample rate of a stream of digital data while introducing only a bounded aliasing error into the data stream (Col 1, L11-13). Therefore, it is obvious to one of ordinary skill in art to implement an integrator interpolating filter of Camp et al. in the digital signal synchronization system of Lew et al, Borazjani et al and Ley et al. By doing so, produce higher sampling rate and reduce cost in high speed digital communication.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eva Y Zheng whose telephone number is 571-272-3049. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eva Yi Zheng  
Examiner  
Art Unit 2611

September 14, 2006

  
CHIEH M. FAN  
SUPERVISORY PATENT EXAMINER